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FIG.1

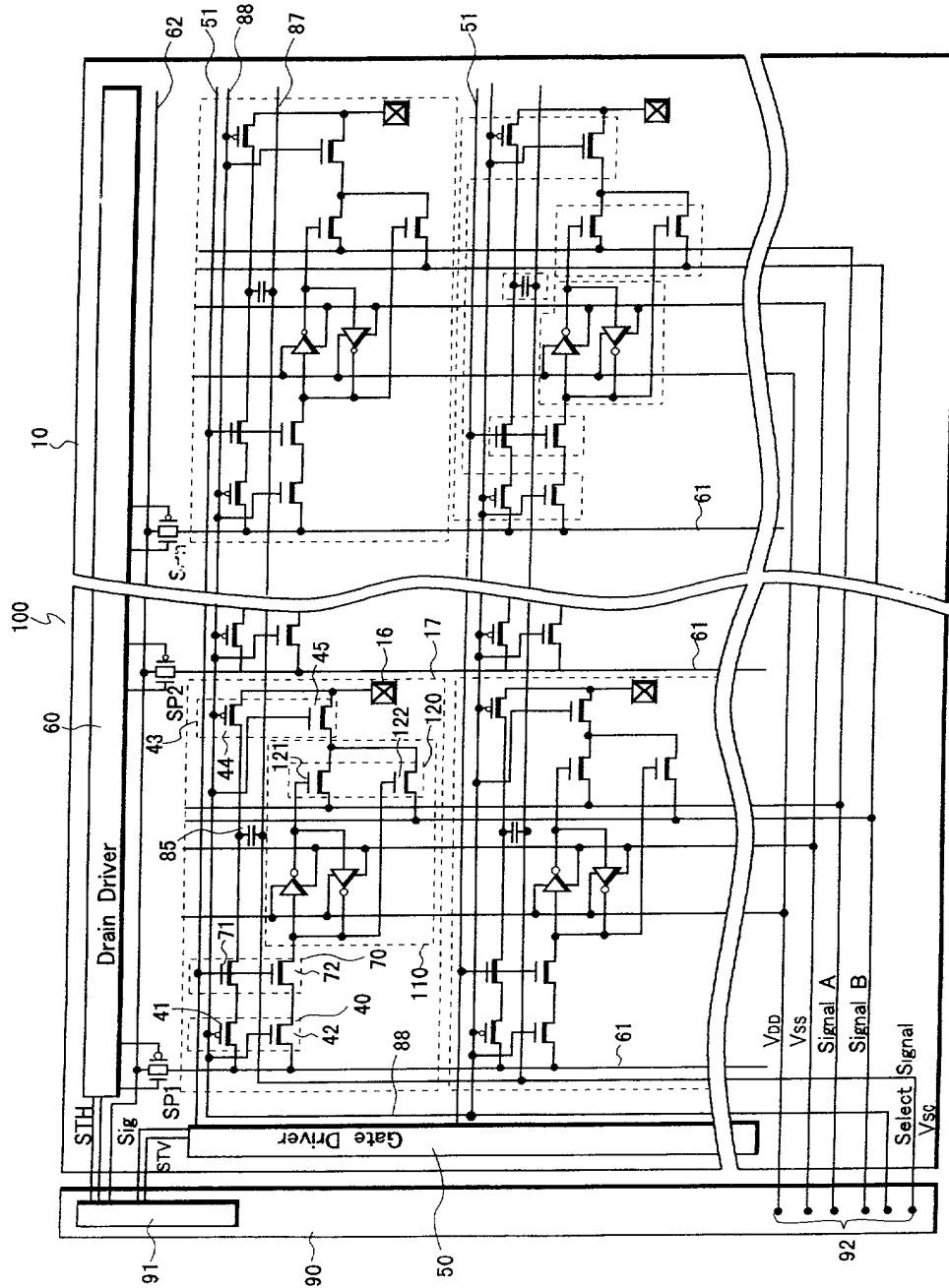
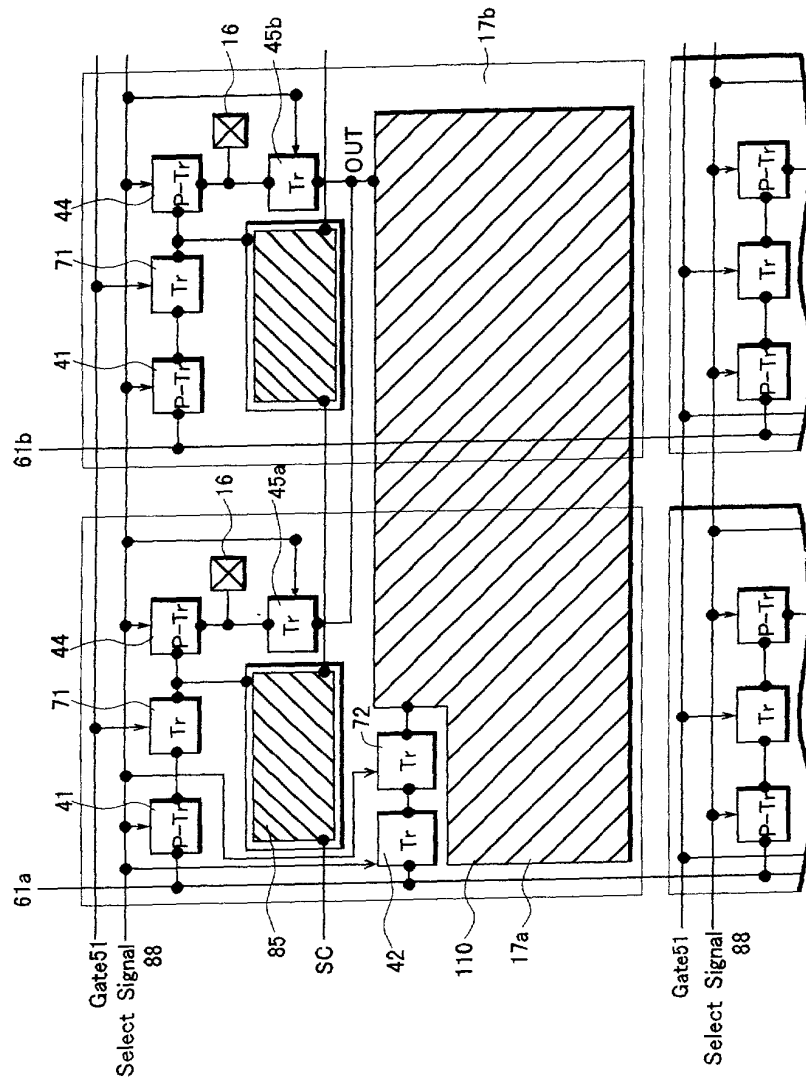


FIG.2

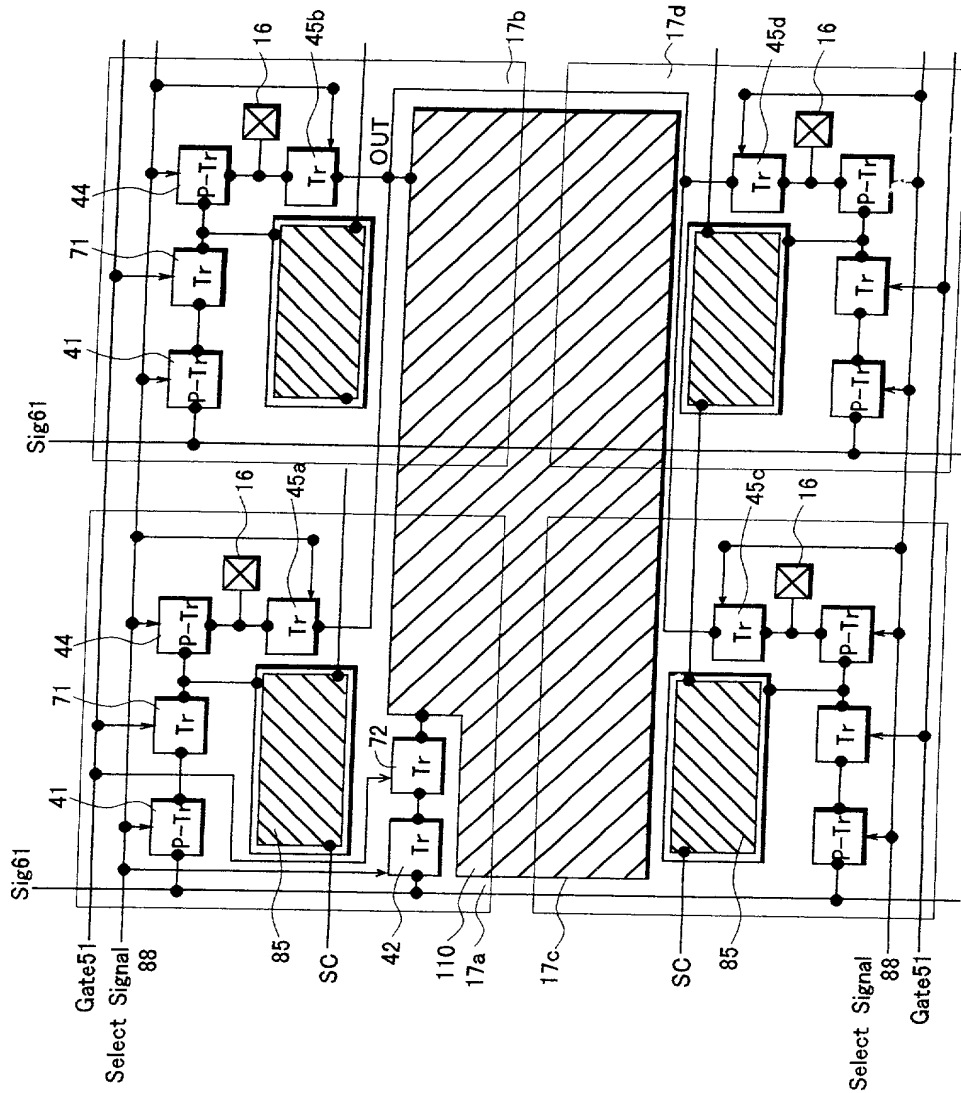
FIG. 2 is a circuit diagram of a memory array element. The diagram is divided into two main sections: a cross-sectional view on the left and a detailed circuit view on the right. The cross-sectional view shows a substrate 110 with a gate stack 17 on top. A select gate 88 is formed on the substrate, and a word gate 51 is formed on the gate stack. A memory cell is formed in the substrate, consisting of a p-type transistor (P-Tr) and an n-type transistor (Tr). The P-Tr is connected to the select gate 88, and the Tr is connected to the word gate 51. The output of the Tr is connected to a bit line 16. The circuit view shows the internal structure of the memory cell. It includes a select gate 88, a word gate 51, and a memory cell 16. The memory cell consists of a p-type transistor (P-Tr) and an n-type transistor (Tr). The P-Tr is connected to the select gate 88, and the Tr is connected to the word gate 51. The output of the Tr is connected to a bit line 16. The circuit view also shows a cross-section of the memory cell, with a p-type transistor (P-Tr) and an n-type transistor (Tr) connected to a select gate 88 and a word gate 51, respectively. The output of the Tr is connected to a bit line 16. The circuit view is labeled with various components: 41, 71, 44, 45, 85, 42, 72, 110, 17, A, and A'.

FIG.4



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FIG.5



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FIG.6

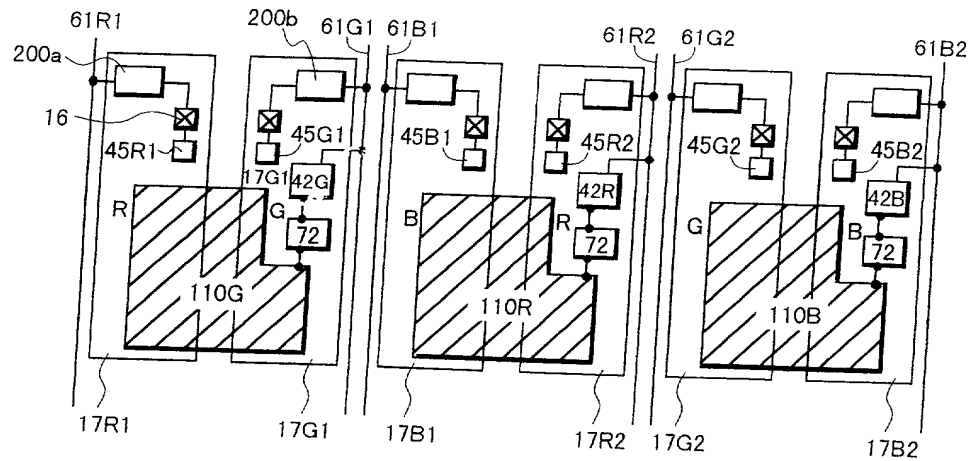
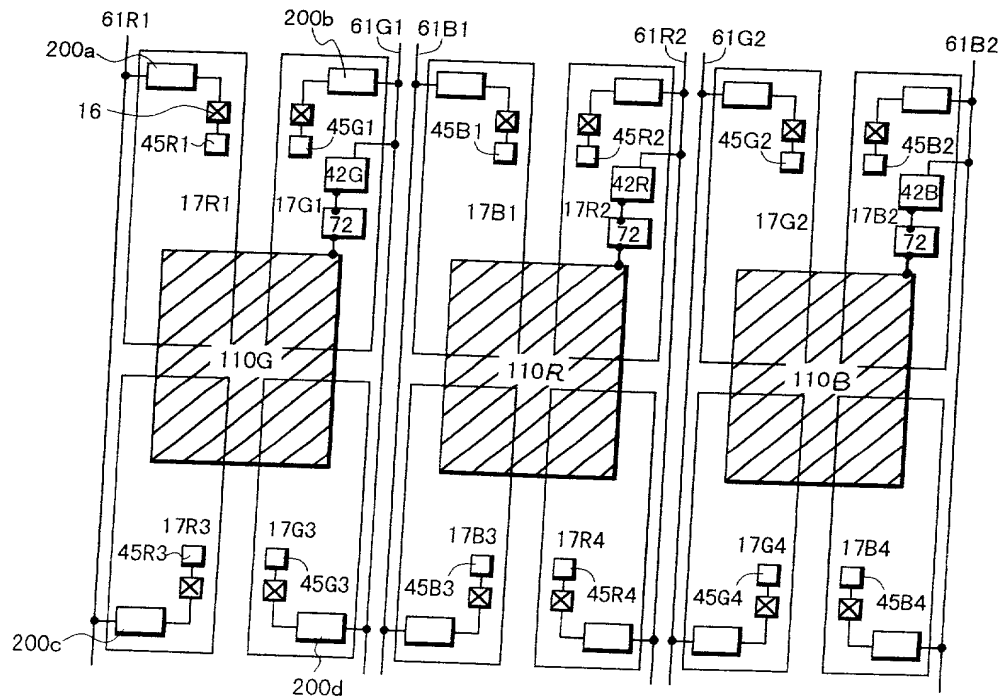


FIG.7



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FIG.8

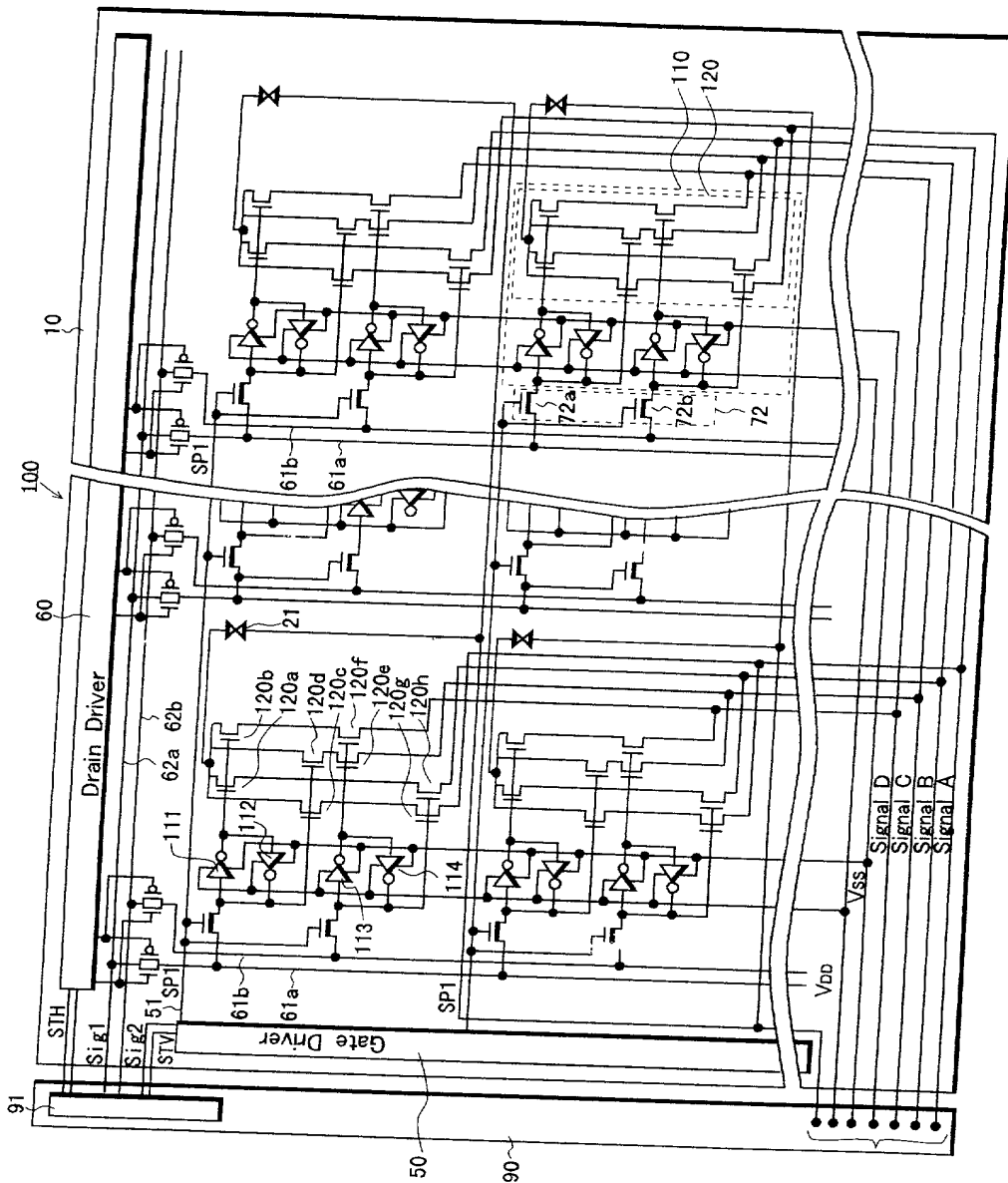


FIG.9

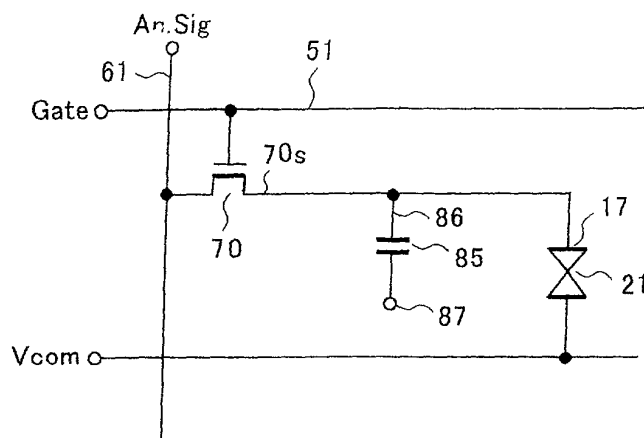
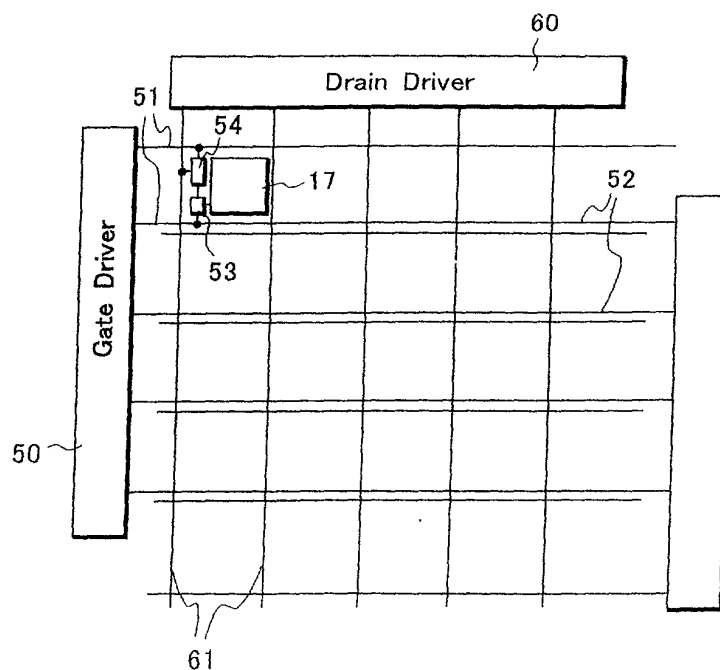


FIG.10



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FIG.11

